ABSTRACT

A content addressable memory (CAM) having a plurality of ternary memory cells, each ternary half cell comprising an equal number of transistors of a p-type and an n-type, the p-type transistors being formed in a first well region and the n-type transistors being formed in a second well region, the wells having at most one p+ to n+ region spacing, the transistors being interconnected to form the half ternary CAM cell and wherein the interconnections for the cell is restricted to a silicon layer and a first metal layer and connections between said cell and external signal lines is restricted to at least a second metal layer.